REMARKS/ARGUMENTS

Reconsideration of this application is respectfully requested.

The Examiner's indication of allowable subject matter at dependent claims 24-29 is appreciatively noted. No further comment will be made with respect to these allowable claims.

In response to the rejection of claim 31 under 35 U.S.C. §112, first paragraph, this claim has been amended so as to be more clearly supported by the originally filed specification. For example, see page 7 in the paragraph just prior to a brief description of the drawings and see also the last paragraph of page 36. As therein noted, those having skill in the relevant art will understand, *inter alia*, that the system may be physically realized in numerous ways, including by the creation of a suitable computer program for running on a conventional computer system. As noted, the computer program can be written in any of a large number of widely used computer programming languages. The original specification specifically noted that the invention provides a carrier medium carrying computer readable code means to cause a computer to execute procedure in accordance with the methods set out, etc.

As now amended, claim 31 is directed to a computer-readable storage medium containing a computer program which, when executed by a computer, carries out the method of claim 16. It is respectfully submitted that such is well within the teaching of

the original specification as viewed through the eyes of those having skill in the relevant art. Accordingly, claim 31 is believed to be adequately supported and well within the requirements of 35 U.S.C. §112, first paragraph.

The apparent rejection of claim 30 under 35 U.S.C. §101 as allegedly directed to non-statutory subject matter is respectfully traversed. However, since this claim has now been cancelled, this ground of rejection has now been mooted and it is not believed necessary to further discuss it.

The rejection of claims 1-12, 16-20, 30-31 and 35-36 under 35 U.S.C. §102 as allegedly anticipated by Jaeckel '507 is respectfully traversed.

Amended claim 1 combines original claims 1, 3 and 4. It now requires that each address decoder identifier has an equal number of bits set to the first selectable state and wherein the means to receive an input address is configured to receive addresses containing a predetermined number of bits set to the first selectable state. That is, the address decoder identifiers are N-of-M codes, where N bits are set to a first selectable state (e.g., 1), and M-N bits are set to a second selectable state (e.g., 0).

Claim 16 has been amended to include the same additional limitations.

Jaeckel uses the architecture originally proposed by Kanerva. In Jaeckel, each memory location can be identified by a subset of S (the set of all possible N-bit binary words), where a subset of S is defined by selecting any ten (or other predetermined

number) of the N coordinates (e.g., bit 37, bit 152, etc.) and assigning a value of either 1 or 0 to that coordinate (e.g., see 9:52-57). The subset of S is the set of all points in S whose values match the assigned values at all ten of the selected coordinates. A random selection of subsets is chosen to be implemented as hard memory locations. Each memory location is addressed by giving the ten selected coordinates and the values of the bits at each of those ten coordinates, each bit having a value of either 1 or 0. An input address will activate a memory location if the values of the bits at the selected ten coordinates of that memory location match the values of the bits at those selected ten coordinates of the input address. that is, if bit 137=1 and bit 157 = 0 for a particular memory location, an input address will only activate that memory location if in that input address, bit 137=1 and bit 157=0. It is necessary to examine both 1s and 0s.

This is in contrast to the method of applicant's claim 1 which requires that the memory include means to activate an address decoder if at least a predetermined minimum number of bits set to the first selectable state in the input address correspond to bits set to the first selectable state in the decoder identifier. In the method of claim 1, the correspondence may occur at any corresponding position of the input address and the decoder identifier which are set to the first selectable state. Jaeckel does not teach correspondence between a predetermined minimum number of bits set to the first selectable state, Jaeckel teaches correspondence between bits at ten predetermined exact coordinates set to either state.

Further, claim 1 requires that each address decoder identifier has an equal number of bits set to the first selectable state and that the means to receive an input address is configured to receive addresses containing a predetermined number of bits set to the first selectable state. As each input address has a predetermined number of bits set to the first selectable state and each address decoder identifier has a predetermined number of bits set to the first selectable state, it is only necessary to match bits having a value of the first selectable state at corresponding coordinates in each address.

Put another way, Jaeckel discloses using binary codes, where it is necessary to select a subset of the input address and look for an exact binary pattern in that subset. In contrast, because applicant's claim 1 uses N-of-M codes (N being the predetermined number set to the first selectable state) for both the address decoder identifier and the input address, it is only necessary to look at the bits set to the first selectable state, thereby improving performance.

Further, while Jaeckel matches an exact binary pattern, the method of claim 1 requires only that a match exceed a predetermined threshold. That is, whereas the method of Jaeckel requires the bits at all ten coordinates to match, the method of claim 1 requires only that the number of correspondences exceeds a predetermined threshold. It is impossible for Jaeckel to teach the number of correspondence exceeding a predetermined threshold, as, in the method disclosed by Jaeckel, only ten correspondences are checked and they must all match.

The Examiner takes the position that Jaeckel teaches each address decoder identifier having an equal number of bits set to the first selectable state. Applicant respectfully disagrees. The Examiner references Jaeckel at 10:35-38 in support of this position. The referenced section of Jaeckel teaches that a memory location is activated by an address if all ten of its assigned values for its ten selected coordinates match the values of the bits at those selected ten coordinates of the input address, as described above.

In particular, the referenced section does not disclose that each address decoder identifier has an equal number of bits set to the first selectable state. Indeed, the referenced section of Jaeckel is silent about address decoder identifiers. As described above, Jaeckel teaches memory locations that are addressed by ten specific coordinates with an address, each having a value of either 1 or 0. The address decoder identifiers are therefore those ten specific coordinates along with the specific values assigned to them, either 1 or 0. In teaching that each memory location is addressed by specific values of 1 or 0 at specific coordinates, Jaeckel is specifically teaching away from each address decoder identifier having an equal number of bits set to the first selectable state.

The Examiner also takes the position that Jaeckel teaches that the means to receive an input address is configured to receive addresses containing a predetermined number of bits set to the first selectable state. The Examiner again references Jaeckel at 10:35-38 in support of this position. However, the referenced section of Jaeckel does not disclose the

means to receive an input address being configured to receive address containing a predetermined number of bits set to the first selectable state. Given that each memory location is addressed by specific bit coordinates having values of either 1 or 0, it will be appreciated that such a condition would be superfluous in the method disclosed by Jaeckel.

with regard to claims 35 and 36, given that Jaeckel fails to teach that the memory includes means to activate an address decoder if at least a predetermined minimum number of bits set to the first selectable state in the input address correspond to bits set to the first selectable state in the decoder identifier, it clearly follows that claims 35 and 36 are not anticipated by Jaeckel for this additional reason.

Given such fundamental deficiencies as already noted, it is not believed necessary at this time to discuss further deficiencies of Jaeckel with respect to other features of the rejected claims. Suffice it to note that, as a matter of law, it is impossible for a reference to anticipate any claim unless it teaches each and every feature of such claim.

The rejection of claim 15 under 35 U.S.C. §102 as allegedly anticipated by Thewes '626 is also respectfully traversed.

Initially, it is noted that in discussing this rejection based on alleged anticipation by Thewes, the Examiner has twice also referred to teachings of Jaeckel. However, since the rejection is based on alleged anticipation by Thewes, the teachings of Jaeckel are

irrelevant. Therefore, the Examiner's comments concerning Jaeckel in this discussion are not believed relevant nor do they require response.

The Examiner appears to be confusing terminology used in Thewes with that used in the present application. For example, the Examiner argues that Thewes teaches use of address decoder neurons. Applicant disagrees. The address decoders as taught by Thewes are not themselves neurons used as address decoders, as is required in claim 15. Rather, the address decoders as taught by Thewes are components within the architecture of a particular neuron. the Examiner's position that the use of input neurons in the present invention reads on neuron inputs in Thewes (Thewes 2:63-C3) is similarly mistaken. The neuron inputs (E1..E4) described in Thewes are the inputs of a particular neuron; they are not themselves neurons. the input neurons of claim 15 are neurons themselves, the outputs of which operate as inputs to the address decoder neurons.

In essence, Thewes describes an implementation of a particular neuron whereas claim 15 is directed to a memory configuration implemented using a neural network, that is, a network of neurons. There is nothing in Thewes to teach or suggest a memory configuration for use in a computer system as recited by claim 15.

The rejection of claims 13-14 under 35 U.S.C. §103 as allegedly being made "obvious" based on Jaeckel in view of Thewes is also respectfully traversed.

Fundamental deficiencies of these references have already been noted with respect to parent claims. Accordingly, it is not believed necessary to discuss the further deficiencies of these references with respect to claims 13-14 at this time.

The rejection of claims 21-23 under 35 U.S.C. §103 as allegedly being made "obvious" based on Jaeckel in view of Ishiriu '595 is respectfully traversed.

The Examiner takes the position that determining on operationally beneficial number of address decoders is inherent in Jaeckel. Applicant respectfully disagrees. As will be appreciated from the arguments provided above in connection with claim 1, Jaeckel teaches that to activate a memory location, all ten selected coordinates must match between the input address and the memory location address. There is therefore no way provided in the method of Jaeckel to affect the number of address decoders that are activated in response to tan input address. How many address decoders are activated is entirely dependent upon whether an input address corresponds with particular memory location addresses at those exact ten coordinates.

This is in contrast to the invention of claim 21 which requires that correspondences between the input address and the decoder identifier exceed a predetermined threshold. This threshold can be altered such that the input address will activate a determined operationally beneficial number of address decoders.

The Examiner argues that Ichiriu teaches configuring the comparison threshold such that a valid input address will activate a number of address decoders substantially equal to the operationally beneficial number of address decoders to be activated. The Examiner refers to 5:17-20 in support of this argument. The Examiner argues that the referenced section of Ichiriu discloses using valid and non-valid words, and the use of a highest priority match register, which only activates the address decoders for the words which generate the highest matches when compared to input addresses. However, it is respectfully submitted that this is not what is disclosed in Ichiriu.

Ichiriu does not teach a plurality of address decoders. Indeed, the method recited by Ichiriu discloses the use of a single address selector 125 which selects a single address from a plurality of address sources. The address selector passes the selected address to an address decoder 127 only a single address decoder is taught, as the address selector 125 only outputs a single address). The address decoder 127 decodes the selected address to activate one of a number of address lines. Further, the address selection described in Ichiriu is based upon the select signal 118 and not upon a comparison between a decoder identified and the input address.

Given that Ichiriu only teaches a single address decoder, and given that the address decoder is not activated based upon a comparison between the decoder identifier and the input address, it clearly follows that Ichiriu could not possibly teach configuring a

comparison threshold (as there is no comparison performed) such that a valid input address will activate decoders to be activated (as there is only one address decoder).

Of course fundamental deficiencies of Jaeckel have already been noted above -- such that it is clear no possible combination of these references could even arguably arrive at the subject matter of independent claim 21 -- let alone the additional features brought by dependent claims therefrom.

The Examiner's attention is also drawn to new claim 37.

New claim 37 is based upon a combination of claims 1, 6, 7 and 9. The Examiner's position seems to be that the feature of claim 6, the use of single bit memories is anticipated by the use of an M-bit word for each memory address as taught by Jaeckel. However, applicant submits that this is not the case.

The memory locations as described by Jaeckel comprise M bit counters (4:34), as in the original method of Kanerva. During a write cooperation, the counters are either incremented or decremented (depending on whether the corresponding bit to be written is a 1 or a 0) until they reach their maximum or minimum values (it is suggested that teach counter have a range of +127 to -127, column 2, paragraph 2). A subsequent read operation adds the corresponding bits of each activated word line into an accumulated word line and applies a threshold to accumulated values to determine which outputs should be set to '1' or '0'.

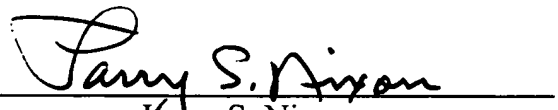
This is in contrast to the method recited by claim 37 which requires that each bit of each word line be stored in single bit memory. An example of what is intended by claim 37 is provided on page 15, paragraph 2 of the present application. The use of single bit memories is possible because the data input line is configured to receive data containing a predetermined number of bits set to the first state. This means that the input data is an N-of-M code, such that it is known how many bits set to the first selectable state should appear in the output data of each read operation (the paragraph bridging pages 13 and 14). As Jaeckel does not teach data having a predetermined number of bits set to the first selectable state, there is no way of knowing how many 1s should appear in the output data, and therefore Jaeckel must use expensive counters to accumulate the data written at each bit of each word line, thereby substantially raising the overall cost of the system.

There is nothing in Jaeckel to teach or suggest that each bit of each word line be stored in single bit memory. Indeed, the method taught by Jaeckel and the use of single bit memories are mutually exclusive, and as such, it is clear there is nothing in Jaeckel that would lead a person skilled in the art to consider the use of single bit memories.

Accordingly, this entire application is believed to be in allowable condition and a formal Notice to that effect is respectfully solicited.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 

Larry S. Nixon
Reg. No. 25,640

LSN:vc
901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000
Facsimile: (703) 816-4100